## REMARKS

The following remarks are made in response to the Office Action mailed November 28, 2003. Claims 1-33 are pending in the present application and stand rejected. The Examiner's reconsideration is respectfully requested in view of the following remarks.

Claims 1-10 and 13 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Cai (U.S. Patent No. 6,501,999). The rejection is respectfully traversed.

The Office Action cites col. 3, lines 25-48 of Cai as anticipating the following in claim 1:

> a scheduler adapted to *schedule* a given task for execution by one of said at least two processing units so as to consume a least amount of energy, and to *reschedule* the given task for execution by an other of said at least two processing units when a determination indicates that said one of said at least two processing units is unable to accommodate execution of the given task based upon the processing requirements of the given task and the corresponding processing capability.

The Office Action further argues that Cai teaches "a scheduler [processor arbitration mechanism], which *attempts to execute tasks* on the power efficient processor, during battery operation mode, *until it is determined that the high-performance is needed* to execute a particular task, such as processing graphic data." Applicant respectfully disagrees and submits that the processor arbitration mechanism of Cai does not operate as the Office Action argues.

It is first noted that the processor arbitration mechanism disclosed in Cai does not execute tasks at all. Cai discloses that the processor arbitration mechanism only "*determines* which processor operates at a given time to provide the required computing power, especially, during the battery operation mode." (Cai, col. 3, lines 25-28). Thus, Applicant assumes that the Examiner meant to argue that the processor arbitration mechanism "schedules tasks to be executed on the power efficient processor, during

battery operation mode, until it is determined that the high-performance is needed to execute a particular task, such as processing graphic data." Even so, Applicant respectfully disagrees.

The cited portion of Cai discloses a processor arbitration mechanism that simply chooses between a "high performance processor" and a "power efficient processor." Cai discloses that the high-performance processor is "powered up to operate when an execution or a series of executions require high-performance operations" and the power-efficient processor is "used to handle operations that are relatively computationally intensive." (Cai, col. 3, lines 28-34). The choice of processors may be made manually by a user through a user interface or automatically through a software application based on predetermined criteria. (Cai, col. 3, lines 35-40).

The argument made by the Office Action that the processor arbitration mechanism schedules the power-efficient processor *until* a determination is made to use the high-powered processor implies that Cai discloses (1) determining to use the power-efficient processor by default, and (2) altering this default determination based on a condition occurring. The cited portion of Cai does not disclose either. As previously noted, the cited portion of Cai discloses a manual (by the user) or automatic (by a software application) selection of either the high-performance or the power-efficient processor for a given time. Cai does not disclose changing this selection for the given time; the processors to be used in other times are selected on their own merit by the processor arbitration mechanism. The cited portion of Cai discloses determining which processor to use only once; it does not disclose determining that the power-efficient processor should be used by default, and then

altering that determination in response to a condition occurring, as the Office Action seems to suggest.

Thus, Applicant respectfully submits that the cited portion of Cai does not disclose "a scheduler adapted to *schedule* a given task for execution by one of said at least two processing units so as to consume a least amount of energy, and to *reschedule* the given task for execution by an other of said at least two processing units when a determination indicates that said one of said at least two processing units is unable to accommodate execution of the given task based upon the processing requirements of the given task and the corresponding processing capability," as claimed in claim 1.

Accordingly, claim 1 is believed to be patentably distinguishable over Cai. Dependent claims 2-10 and 13 are believed to be allowable for at least the reasons given for claim 1. Withdrawal of the rejection of 1-10 and 13 under 35 U.S.C. §102(e) is respectfully requested.

Claims 11-12 and 14-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Cai in view of Inoue (U.S. Patent No. 4,954,945). The rejection is respectfully traversed.

Regarding independent claim 14, Inoue teaches *checking* flag registers of processors and entries in a task table to determine which processor is available and most efficient, respectively, to perform a specified task. (Inoue, col. 3, lines 39-61). Inoue does not teach or suggest, as the Office Action argues, "*querying* said plurality of processing units," as essentially claimed in claim 14. Further, by only *checking* flag registers and entries in a task table, the processors taught by Inoue cannot, in response to the *query*, "one of *accept* and *reject* the execution of the given task," as essentially claimed in claim 14.

That is, the processors taught by Inoue do not perform a step of accepting or rejecting a query. Thus, the combination of Cai and Inoue does not teach or suggest "a scheduler adapted to schedule a given task for execution by one of said plurality of processing units by querying said plurality of processing units in a partial order of descending energy efficiency to one of accept and reject the execution of the given task until one of the given task is one of accepted and executed by said one of said plurality of processing units and the given task is rejected by all of said plurality of processing units," as claimed in claim 14.

Independent claim 24 contains at least the limitations of claim 1. Accordingly, the combination of Cai and Inoue does not teach or suggest at least the limitations addressed in more detail above for claim 1. Further, the combination of Cai and Inoue does not teach or suggest "at least two processing units...adapted to one of *accept* and *reject* scheduled tasks based upon processing requirements of the scheduled tasks and a corresponding processing capability," as essentially claimed in claim 24, and addressed in more detail above for claim 14.

Regarding claim 31, the Office Action does not address, and the combination of Cai and Inoue does not teach or suggest, "a processor attribute table adapted...to update the processing capability information *dynamically* when the processing capability information changes," as essentially claimed in claim 31.

Accordingly, claims 14, 24 and 31 are believed to be patentably distinguishable and nonobvious over Cai in view of Inoue. Dependent claims 11-12, 15-23, 25-30, and 32-33 are believed to be allowable for at least the reasons at least the reasons given for claim 1,

14, 24 and 31. Withdrawal of the rejection of 11-12 and 14-33 under 35 U.S.C. §103(a) is respectfully requested.

In view of the foregoing remarks, it is respectfully submitted that all the claims now pending in the application are in condition for allowance. Early and favorable reconsideration is respectfully requested.

Respectfully submitted,

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